COURSE PROGRAM

Academic Year: 2022/2023

Identification and characteristics of the course			
Code	501086	ECTS Credits	6
Course name (English)	Analog Electronics		
Course name (Spanish)	Electrónica Analógica		
Degree programs	Degree in Electronic and Automatic Engineering (Industrial Branch) Degree in Mechanical Engineering (Industrial Branch)		
Faculty/School	School of Industrial Engineering		
Semester	6th	Type of course	Compulsory
Module	Specific technology for industrial electronics and automation Eligibility		
Matter	Electronics Diversification in Industrial Electronics and Automatic Engineering		
Lecturer/s			
Name	Office	E-mail	Web page
Raquel Pérez-Aloe Valverde	D1.3	raquel@unex.es	http://campusvirtual.unex.es/
Subject Area	Electronic Technology		
Department	Electrical, Electronic and Automatic Engineering		
Coordinating Lecturer (Ifmore than one)	Raquel Pérez-Aloe Valverde		

Competencies (see tableathttp://bit.ly/competenciasGrados)

Basic Competences	Check With an " X"	General Competences	Check With an " X"	Transversal Competences	Check With an " X"	Specific Competences Basic Formation	Check With an " X"	Specific Competences Common to the Industrial Branch	Check With an " X"	Specific Competences Specific Technology	Check With an " X"	Specific Competences Specific Technology	Marcar con una " X"
CB1		CG1	X	CT1	X	CEFB1		CECRI1		CETE1		CETE11	
CB2		CG2	X	CT2	X	CEFB2		CECRI2		CETE2	X	CETE12	
CB3		CG3	X	CT3	X	CEFB3		CECRI3		CETE3		CETE13	
CB4		CG4	X	CT4	X	CEFB4		CECRI4		CETE4		CETE14	
CB5		CG5	X	CT5	X	CEFB5		CECRI5		CETE5		CETE15	
		CG6	X	CT6	X	CEFB6		CECRI6		CETE6	X	CETE16	
		CG7	X	CT7	X			CECRI7		CETE7		CETE17	
		CG8	X	CT8	X			CECRI8		CETE8		CETE18	
		CG9	X	CT9	X			CECRI9		CETE9		CETE19	
		CG10	X	CT10	X			CECRI10		CETE10		CETE20	
		CG11	X					CECRI11				CETFG	
		CG12						CECRI12					

Contents

Course outline

Design, specifications and applications of analog circuits.

The course is structured in the following thematic blocks:

- **Simple Gain Stages (Lessons 1 and 2):**

  In this thematic block the student reviews the operation mode and modelling of the bipolar and MOS transistors as well as its use in the configuration of the simplest gain stages. Also, the student will become familiar with the methodology to analyze the influence of the different capacitances (physical and parasitic) in the frequency response of the different analog circuits.

- **Basic Analog Electronic Circuits (Lessons 3 and 4):**

  In these units, the electronic blocks that allow the design of more complex analog circuits are studied, starting from the simplest amplifying structures already analyzed.

- **Feedback (Lesson 5):**

  The goal of this unit is to make the general structure of a feedback circuit, the advantages and disadvantages of this structure and the guidelines for the analysis of this type of circuit known to the students. Different structures with Operational Amplifiers will be analysed.

Course syllabus

Title of lesson 0: Introduction to the course

Contents of lesson 0:

0.1 Organization of the course
0.2 Course assessment methods
0.3 Resources and materials
0.4 Review of background knowledge

Title of lesson 1: Single stage amplifiers

Contents of lesson 1:

1.1 Concept of amplifier gain, transfer characteristic, operating point, voltage, current and power amplifiers. Efficiency
1.2 Concepts of small signal and large signal operation. Concept of distortion
1.3 Biasing networks
1.4 Basic structures, high and low impedance terminals
1.5 Common emitter (source), base (gate), collector (drain) amplifier stages

Description of practical activities for lesson 1:

L.1 Lab 1: BJT common emitter, common base or common collector amplifier stage. Experimental session in Laboratory D.1.17. (2 h)

LD.1 Design project session 1. Experimental session in Laboratory D.1.17 (2 h)

Title of lesson 2: Frequency response

Contents of lesson 2:

2.1 Signal frequency spectrum
2.2 Amplifier transfer function
2.3 Frequency response of a single-time-constant network
2.4 Concept of dominant and secondary pole

2.5 Low and high frequency dominant pole approximation: short-circuit and open-circuit time constants
2.6 Frequency response of amplifiers

Description of practical activities for lesson 2:

L.2 Lab 2: BJT common emitter, common base or common collector amplifier stage. Frequency response. Experimental session in Laboratory D.1.17. (4 h)

LD.2 Design project session 2. Experimental session in Laboratory D.1.17 (2 h)

Title of lesson 3: Output stages

Contents of lesson 3:

3.1 Concept of power amplifier: requirements
3.2 Operation in class A, B and class AB
3.3 Transfer curves, power dissipation and efficiency

Description of practical activities for lesson 3:

LS.1 Sim 1: Output stages in class A, B and AB. Simulation session in Laboratory D.1.17. (2 h)

LD.3 Design project session 3. Experimental session in Laboratory D.1.17 (2 h)

Title of lesson 4: The differential pair

Contents of lesson 4:

4.1 BJT and MOS structure, operation mode and large signal analysis
4.2 Response to differential signals, differential gain, offset and mismatching
4.3 Response to common signals, CMRR concept, common mode input range (CMR)
4.4 Differential pair with active loads

Description of practical activities for lesson 4:

LD.4 Design project session 4. Experimental session in Laboratory D.1.17 (2 h)

LD.5 Design project session 5. Experimental session in Laboratory D.1.17 (2 h)

Title of lesson 5: Feedback

Contents of lesson 5:

5.1 General structure and analysis of a feedback system. Advantages and disadvantages of feedback
5.2 Analysis of different configurations with Operational Amplifiers
5.3 Effect of feedback on system poles, instability and compensation

Description of practical activities for lesson 5:

LD.6 Design project session 6. Experimental session in Laboratory D.1.17 (2 h)

LD.7 Design project session 7. Experimental session in Laboratory D.1.17 (2,5 h)

Educational activities

Student workload in hours by lesson		Lectures	Practical activities				Monitoring activity	Homework
Lesson	Total	L	HI	LAB	COM	SEM	SGT	PS
0	6	1		0	0		0	5
1	30,5	6		4	0		0,5	20

2	21,5	5		6	0		0,5	10
3	19,5	3		4	0		0,5	12
4	31,5	6		4	0		1	20,5
5	23	6		4,5	0		0,5	12
Assessment[1]								
Ass. Act. 1								
Ass. Act. 2								
...								
Final Assessm.	18	3		0	0			15
TOTAL	**150**	**30**		**22,5**	**0**		**3**	**94,5**

L: Lectures (100 students)
HI: Hospital internships (7 students)
LAB: Laboratory or field practices (15 students)
COM: Computer room or language laboratory practices (30 students)
SEM: Problem classes or seminars or case studies (40 students)
SGT: Scheduled group tutorials (educational monitoring, ECTS type tutorials)
PS: Personal study, individual or group work and reading of bibliography

Teaching Methodologies

Among the teaching methodologies included in the formative program, in this course the following are used:

Teaching methodology	Used methodologies labelled as "X"
1. Explanation and discussion of theoretical contents.	X
2. Resolution, analysis and discussion of support examples or previously proposed exercises.	X
3. Exposition of related topics by students.	X
4. Development of case studies or demonstrations at laboratory, computer room, etc.	X
5. Resolution of specific doubts in small groups in order to identify potential problems in the teaching-learning process, and academic guidance for essays, case studies, practical works, demonstrations, etc.	X
6. Search for information prior to the development of the topics, or for complementary information once they are in progress.	X
7. Preparation of essays, either individually or in groups.	X
8. Study of each topic, which may consist of: content study, analysis of practical exercises or case studies, preparation for examinations, etc.	X

The **Lectures** will be developed in a previously assigned classroom. The resources and teaching material, available in advance in the space reserved for the course in the Virtual Campus of the UEx, will be used. The explanations of those contents that are either new to the student, or could have some difficulty, will be discussed in detail on the blackboard.

Regarding the **lab activities**, these have been divided into three different types of activities:

1. **L1-L2** are experimental sessions where each group of students must design an BJT amplifier fulfilling some requirements regarding the voltage gain and the bandwidth. These lab sessions take place in laboratory D.1.17, and will consist of the theoretical analysis, simulation using CAD tools (OrCAD 16.6 32b or OrCAD 17.2 64b in their LITE versions for students), assembly and test of the gain stages

studied in theoretical classes. Before the beginning of the lab sessions, the student must present a form (*prelab*) about the content to be developed in the laboratory. Once finished the lab session, the student group will have to submit to evaluation a report with the analysis of the experimental results obtained. Because the groups are formed by two students, this activity, as well as allowing the acquisition of the own competences of the degree mentioned above, contributes to the acquisition of those related to the block of transversal competences established by *ENAEE:*

6.1 (CTE1) - Work effectively both individually and as a team.

6.2 (ETC2) - To use different approaches to communicate effectively with the engineering community and with society in general.

2. **LS1** is a simulation session to study the behaviour of the different classes of output stages. The main aim is to analyse in depth concepts already discussed in the theoretical classes, using CAD simulation tools freely accessible to students, then making them aware of the commitment with professional ethics and working, in part, the transversal competence 6.3 of ENAEE related to,

   6.3 (ETC3) - Demonstrate awareness of responsibility for the practical application of engineering, social and environmental impact, and commitment to professional ethics, responsibility and standards in the practical application of engineering.

3. **LD1-LD7** are dedicated to developing design projects of electronic circuits that are useful in the environment of industrial electronic engineering. This activity is carried out by groups of students previously configured (usually groups of 3 students). In this way, these sessions allow to perform a **Project Based Learning (*PBL*) methodology** that is very appropriate for engineering students. At the end of the project, each group of students must submit a report and make an oral presentation showing the prototype functionality. In addition to the competences of the degree that are attained with this type of activity, the corresponding transversal competences of ENAEE CTE1 and CTE2 described above would also be acquired.

The **Monitoring activities** will be developed within the timetable assigned by the Centre to the programmed tutoring.

Learning outcomes

- Understand the operation of electronic components in linear operation.
- Know, understand, and analyse the operation of the different fundamental blocks that form the basis of the electronic design and the factors that have an impact on their performance.
- Learn the concepts of gain, frequency response and feedback in amplifiers.
- Show the influence of the different capacitances (physical and parasitic) on the frequency response of the different electronic circuits.
- Identify the different feedback topologies and analyse their influence on the circuit performance identifying their advantages and disadvantages.
- Know how to use operational amplifiers and some of their applications.

Assessment systems

Assessment criteria:

CRI1. Proficiency in the use of the CAD tools used in practical sessions.

Related to the competences CB5, CG3, CT5, CETE2, CETE6.

CRI2. Know to solve the proposed problems, applying the knowledge acquired in lessons.

Related to the competences [CB1-CB3], [CG4-CG9], CG11, [CT1-CT2], CT4, CT6, [CT8-CT10], CETE2, CETE6.

CRI3. Know how to communicate and transmit their knowledge with an appropriate technical language within the field of analog electronics.

Related to the competences [CB1-CB4], [CG1-CG2], [CG9-CG11], [CT3-CT4], [CT6-CT9], CETE2, CETE6.

CRI4. Have acquired skills related to the analysis of an analog electronic circuit by simple inspection, by the resolution of equivalent circuits, by simulation using CAD tools and/or by implementation and test in the laboratory.

Related to the competences [CB1-CB5], [CG3-CG11], [CT1-CT2], [CT4-CT6], CT10, CETE2, CETE6.

Assessment activities:

Among the assessment activities included in the formative program, in this course the following are used:

	Range fixed	Ordinary call	Extraordinary call	Global assessment
1. Final exam and/or partial examinations.	0%–80%	60%	60%	60%
2. Practical activities in: classroom, lab, computers room, visits, etc	0%–50%			
3. Solution and submission of activities (cases, exercises, assignments, projects, etc.), individually and/or in groups	0%–50%	40%	40%	40%
4. Active participation in the learning activities.	0%–10%			
5. Attendance to the learning activities.	0%–10%			

Description of the assessment activities:

Students selecting continuous assessment

Assessment activity 1.-Final examination

- A single **final exam** will be taken, consisting of the resolution of theoretical questions and problems regarding the topics explained in the course.
- It will contribute to the final grade in a **60%.**
- It will be evaluated on a **maximum grade of 10.**
- It will be compulsory to achieve a **minimum grade of 4 out of 10** in order to compute the grades of the rest of the activities. If this minimum grade is not achieved and, nevertheless, the total calculation of the grade exceeds the mark of 5 out of 10, the final grade that will appear in the **academic transcript will be 4.5.**
- This is a **REPEATABLE** activity.

Assessment activity 2.-Solution and submission of activities

2.1 Submission of practical reports:

- **The reports** should include the results of the work carried out during the practical laboratory activities.
- It will contribute to the final grade in a **20%.**
- It will be evaluated on a **maximum grade of 10.**
- The student may be asked **to complete a form** about the contents of the activity before the beginning of it.
- To be able to submit the report**, it is compulsory** to have attended the lab sessions, being allowed to miss only one of them in a justified way.
- In the case that a student has not attended the lab sessions, in order to pass the course, he will **have to take a practical exam**. The grade will be passed/failed.
- This is a **NON-REPEATABLE** activity.

2.2 Submission and presentation of a project:

- During the course, the student will be asked to develop and present an **electronic design project.**
- It will contribute to the final grade in a **20%.**
- It will be evaluated on a **maximum grade of 10.**
- This is a **REPEATABLE** activity.
- The student who has passed the course in the ordinary call without submitting and presenting the project, may do so in the extraordinary call in order to improve his grade. In this case, the final grade that will appear in academic transcript of the ordinary call will be 4.5. The grades obtained in the ordinary call corresponding to the assessment activities 1 and 2.1 will be kept in the extraordinary call.

Students selecting global assessment

The global assessment will take place the same date as the final examination associated to the "continuous assessment" and will consist of the two following activities:

Assessment activity 1.-Final examination

- A single **final exam** will be taken, consisting of the resolution of theoretical questions and problems regarding the topics explained in the course.
- It will contribute to the final grade in a **60%.**
- It will be evaluated on a **maximum grade of 10.**
- It will be compulsory to achieve a **minimum grade of 4 out of 10** in order to compute the grades of the rest of the activities. If this minimum grade is not achieved and, nevertheless, the total calculation of the grade exceeds the mark of 5 out of 10, the final grade that will appear in the **academic transcript will be 4.5.**
- This is a **REPEATABLE** activity.

Assessment activity 2.- Practical examination

- This activity will consist of a test that will evaluate, on the one hand, the acquisition of skills related to the lab activities carried out throughout the course **(20%)** and on the other hand, the student's ability to develop an electronic design project **(20%).**
- It will be evaluated on a **maximum grade of 10.**
- This is a **NON-REPEATABLE** activity.

Bibliography (basic and complementary)

Basic Bibliography:

1. A. S. Sedra and K. C. Smith, Microelectronics Circuits (7/e), Oxford University Press, 2015.
2. B. Razavi, Fundamentals of Microelectronics, (2/e), Wiley 2012.
3. M. H. Rashid, Microelectronic Circuits: Analysis and Design, (2/e), Cengage Learning, 2010.

Complementary Bibliography:

4. A. Malvino, Principios de Electrónica (7/e), McGraw Hill, 2007.
5. A. R. Hambley, Electrónica (2/e), Prentice Hall, 2002.

Other resources and complementary educational materials

Available in the Virtual Campus of the University of Extremadura

http://campusvirtual.unex.es/zonauex/avuex/course/view.php?id=13551